REMARKS

Claims 1-10 remain pending in the above-identified application. Claims 1, 9, and 10 are amended. No claims are canceled or added. A substitute specification is provided and the abstract is amended to address informalities.

Before addressing specifically the individual issues raised in the Office Action, applicants summarize an aspect of the disclosed invention. In particular, applicants note that a purpose of the invention is to use as much material as possible of a "predetermined manufacturing block" to form "printed wiring boards." More specifically:

When forming printed wiring boards of a single type, naturally a single predetermined manufacturing block is partitioned to accommodate as many of the printed wiring boards as possible. Additional predetermined manufacturing blocks are used as necessary until enough printed wiring boards are formed to fulfill the order requirements. Often, the last batch of printed wiring boards of the order will not use a predetermined manufacturing block to its full capacity, and the remainder of the predetermined manufacturing block will be wasted, unless it is used also for printed wiring boards of another type and/or from another order.

By implementing the present invention, data for the ordered printed wiring boards is stored and processed to determine efficient use of the predetermined manufacturing blocks. To describe applicants' invention in more detail, the present application uses the terms "non-fractional" and "fractional" as follows: If a group of printed wiring boards formed from a single predetermined manufacturing block are all of the same type, these boards are labeled "non-fractional" printed wiring boards. If a group of printed wiring boards formed from a single predetermined manufacturing block are not all of the same type, these boards are labeled "fractional" printed wiring boards.

As explained in more detail below, applicants' invention is distinguishable from the asserted prior art for at least the reason of its differing detecting unit or its differing detecting of a plurality of fractional printed wiring boards. More specifically, applicants' manufacturing system is embodied in a CPU 31 and a recording medium 32, which includes a single piece drawing number data library 35 storing printed wiring board data and a panelizing data library 34 storing predetermined manufacturing block data. Also, applicants' manufacturing method includes the detecting of fractional printed wiring boards using the CPU 31 and the recording medium 32, which includes the single piece drawing number data library 35 storing printed wiring board data and the panelizing data library 34 storing predetermined manufacturing block data. Further, applicants' computer-readable recording medium stores a computer program that detects fractional printed wiring boards using the CPU 31 and the recording medium 32, which includes the single piece drawing number data library 35 storing printed wiring board data and the panelizing data library 34 storing predetermined manufacturing block data. (See applicants' specification, from page 11, line 24, to page 12, line 23, and Fig. 3.)

As discussed in applicants' specification, from page 17, line 7, to page 18, line 4, the detecting unit or step of detecting is realized in one embodiment by the CPU 31, which performs the following processes as step S103 in Fig. 6:

(1) predetermined manufacturing block data are read out from the recording medium 32;

(2) data of a certain type (or "kind") of ordered printed wiring board are read out from the recording medium 32; and

(3) printed wiring boards are virtually laid out on the predetermined manufacturing block according to the quantity ordered.

The processes (1) – (3) are carried out for each type of ordered printed wiring board.

In the process (3) above, the printed wiring boards of a specified type (based on read-out printed wiring board data) are laid out as many as possible, in a single virtual predetermined manufacturing block based on the predetermined manufacturing block data. When the number of the ordered printed wiring boards exceeds the maximum number of the printed wiring boards that can be laid out in the single predetermined manufacturing block, additional virtual predetermined manufacturing blocks are prepared as required. At that time, there may be a case where the printed wiring boards laid out in the final batch (in an additional predetermined manufacturing block) are in a number smaller than the above-mentioned maximum number. In such a case, the respective printed wiring boards of the same type, which were laid out in each non-final virtual predetermined manufacturing block, are labeled as "non-fractional printed wiring boards." On the other hand, the respective printed wiring boards, which are laid out in the final batch, are labeled as "fractional printed wiring boards."

Fig. 7 shows an example of the fraction processing of step S103, in which ten virtual pieces of the ordered printed wiring boards labeled "E320-1234-T567/01" are laid out in three virtual predetermined manufacturing blocks. In this example, a maximum of four pieces of the printed wiring boards can be laid out in a single predetermined manufacturing block. Therefore, two additional predetermined manufacturing blocks are prepared for laying out all ten of the printed wiring boards. On the third predetermined manufacturing block (the right-hand block in the drawing), which corresponds to the final batch, the final two printed wiring boards are laid out. The detecting unit detects (labels) these two printed wiring boards as "fractional printed wiring boards." Further, in Fig. 7, the printed wiring boards which are laid out in the first (the left-hand block in the drawing) and second (the middle block in the drawing) predetermined

manufacturing blocks, are labeled "non-fractional printed wiring boards." Such fraction processing is neither taught nor suggested by the asserted prior art.

Applicants now respond to the individual issues raised in the Office Action.

Claims 1, 9, and 10 stand rejected under 35 U.S.C. § 112, second paragraph, as indefinite. In view of the following, applicants submit that the rejection should be withdrawn:

The Office Action indicates on page 2 that it is unclear what a "fractional printed circuit board" is. Apparently, the reference is to "fractional printed *wiring* board," as recited in the claims. As applicants explain above, if a group of printed wiring boards formed from a single predetermined manufacturing block are not all of the same type, these boards are labeled "fractional printed wiring boards." The claims recite that the fractional printed wiring board is to be laid out to a format of a single predetermined manufacturing block together with a plurality of printed wiring boards having a different type within the printed wiring boards scheduled to be manufactured. In view of this explanation, applicants respectfully submit that the term "fractional printed wiring board" would be sufficiently clear to one skilled in the art.

The Office Action also states that it is unclear what a "detecting unit" is. Specifically, it is questioned whether it is a physical sensor or software. Applicants respond that the detecting unit of the present invention is not a physical sensor but is embodied instead in a CPU and a recording medium that stores software. Note for example CPU 31 in Figs. 3 and 5 and recording medium 32 in Fig. 3. Also, Fig. 6 represents the software process of the detecting unit as step S103. Additionally, note the discussion in applicants' specification from page 17, line 7, to page 18, line 4.

Lastly, it is apparently inquired if the "determining unit" judges whether to use particular portions of the predetermined manufacturing block to form the ordered printed wiring boards. The determining unit does provide this judgment.

In view of the explanations above, applicants now solicit the withdrawal of the indefiniteness rejection.

Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as obvious over Kitamura (U.S. Patent No. 6,223,093) in view of Kalagnanam et al. (U.S. Patent No. 6,044,361). Applicants respectfully traverse this rejection as unjustified.

For example, each claim recites (explicitly or by virtue of its dependency from another claim) a step of detecting or a detecting unit that performs the step of detecting the following:

> a plurality of fractional printed wiring boards ... to be laid out to a format of[1] a single predetermined manufacturing block together with a plurality of printed wiring boards having a different type ...

The Office Action indicates (page 3, paragraph b) that the Kitamura equipment information memory 205 detects the plurality of fractional printed wiring boards as described in the claims. However, a memory cannot perform a function, so certainly it cannot perform the claimed function.

The Office Action also cites multiple memory modules illustrated in the Kitamura Fig. 11 along with a network and an element labeled "semiconductor device manufacturing equipment 1110." However, memory modules and the network cannot perform the function cited above. Regarding semiconductor device manufacturing equipment 1110, the Office Action does not elaborate, except to cite column 8, lines 36-67, and to say that Kitamura at least implies that the claim detection occurs. Regarding the cited text, applicants find no statement showing that any

[1] Previously, claim 10 was inadvertently not amended analogously to how claims 1 and 9 were amended, that is, to recite "a format of." For consistency, this phrase is now added to claim 10.

of the cited prior art memory modules, the network, or semiconductor device manufacturing equipment 1110 anticipates the function quoted above that is recited in the claims.

Therefore, the rejection has not been justified for at least the reason that no explanation is provided of how the prior art supposedly teaches (or even suggests) a step of detecting or a detecting unit that performs the step of detecting as specifically described in the claims.

Further, even if such an explanation is subsequently provided, to justify a rejection of the pending claims, an additional explanation would now be required that supposedly explains how Kitamura or Kalagnanam et al. teaches or suggests the step of detecting or a detecting unit that performs this step by, for each type of ordered printed wiring board: (1) reading out predetermined manufacturing block data from a panelizing data library; (2) reading out data of a certain type of ordered printed wiring board from a single piece drawing number data library; and (3) virtually laying out the printed wired boards on the predetermined manufacturing block according to the quantity ordered. Applicants submit that neither Kitamura nor Kalagnanam et al. teaches or suggests the claimed detection.

Accordingly, applicants solicit the withdrawal of the anticipation rejection based on Kitamura and Kalagnanam et al.

Claims 7 and 8 stand rejected under 35 U.S.C. § 103(a) as obvious over Kitamura in view of Kalagnanam et al., and further in view of Shin et al. (U.S. Patent No. 6,295,728). This rejection should be withdrawn for at least the following reason:

Claims 7 and 8 depend from claim 1. Therefore, because the rejection of claim 1 based on Kitamura and Kalagnanam et al. should be withdrawn, the rejection of claims 7 and 8 should also be withdrawn for at least the reason of their dependency. Applicants acknowledge that,

unlike for base claim 1, claims 7 and 8 are also rejected based in part on Shin et al. However, Shin et al. is not relied upon to teach or suggest the features recited in claim 1.

Accordingly, applicants now solicit the withdrawal of the obviousness rejection of claims 7 and 8.

Claim 1 stands rejected under 35 U.S.C. § 103(a) as obvious over Dighe et al. (U.S. Patent No. 5,815,398) in view of Kitamura. Applicants respectfully traverse this rejection as unjustified.

As noted above, claim 1 describes a manufacturing system that includes:

> a detecting unit detecting a plurality of fractional printed wiring boards ... to be laid out to a format of a single predetermined manufacturing block together with a plurality of printed wiring boards having a different type ...

The Office Action does properly explain how Dighe et al. supposedly teaches or suggests a manufacturing system having this element.

To show how Dighe et al. supposedly teaches the placement of printed wiring boards on a single predetermined manufacturing block, the Office Action provides citations to column 4, lines 62-65, computer steps 59 and 61, and a part sequence 54. Applicants address each of these citations as follows:

Regarding column 4, lines 62-65, this text discusses circuit components to be arranged compactly within a region instead of printed circuit boards to be formed from a single predetermined manufacturing block as described in claim 1. Although some may think that the goal of the invention is analogous to the discussion of efficiently cutting shapes from fabric, leather, sheet metal, steel, thermal insulation, and closed cell or open cell foam or foam type padding as disclosed by Dighe et al. (see column 4, lines 58-62), the Office Action does not state that the rejection relies on the above-identified claim feature as being an obvious variant of the

subject matter taught by Dighe et al. Instead, the rejection is based on a belief that Dighe et al. teaches the claim feature.

Regarding the cited computer steps, Fig. 3A shows that step 59 is merely identifying a set of parts and step 61 is an inquiry if more parts need the assignment of bias values (note step 60). Surely, this disclosure is not sufficient to teach the detection of a plurality of fractional printed wiring boards with the details described in claim 1.

Regarding the part sequence 54, the Office Action does not explain how a part sequence, arbitrarily generated (see column 7, lines 28-33), supposedly anticipates a detecting unit that detects a plurality of fractional printed wiring boards that should be laid out as specifically described in the claim.

For at least the reason that the Office Action does not properly explain how Dighe et al. supposedly teaches the claimed detecting unit, the rejection is not justified. Applicants of course acknowledge that the rejection also relies on Kitamura, but Kitamura is not relied upon to teach or suggest this element.

Further, even if it could be explained how Dighe et al. or Kitamura supposedly teaches or suggests the claimed detecting unit, to justify a rejection of the pending claims, an additional explanation would now be required that supposedly explains how Dighe et al. or Kitamura teaches or suggests a detecting unit that carries out the detection by, for each type of ordered printed wiring board: (1) reading out predetermined manufacturing block data from a panelizing data library; (2) reading out data of a certain type of ordered printed wiring board from a single piece drawing number data library; and (3) virtually laying out the printed wired boards on the predetermined manufacturing block according to the quantity ordered. Applicants submit that neither Dighe et al. nor Kalagnanam et al. teaches or suggests this claimed detection.

Accordingly, applicants solicit the withdrawal of the obviousness rejection based on Dighe et al. and Kitamura.

Claim 1 stands rejected under 35 U.S.C. § 103(a) as obvious over Blaimschein (U.S. Patent No. 5,953,232) in view of Kitamura. Applicants respectfully traverse this rejection as unjustified.

As noted above, claim 1 describes a manufacturing system that includes:

> a detecting unit detecting a plurality of fractional printed wiring boards ... to be laid out to a format of a single predetermined manufacturing block together with a plurality of printed wiring boards having a different type ...

The Office Action does properly explain how Blaimschein supposedly teaches or suggests a manufacturing system having this element. (Although the rejection also relies on Kitamura, this reference is not relied upon to teach or suggest the above-quoted claim element.) Accordingly, the rejection is not justified. Applicants elaborate as follows:

First, applicants respectfully disagree with the statement in the Office Action, page 13, first full paragraph, that Blaimschein concerns a manufacturing process for cutting printed circuit boards. Applicants have searched the Blaimschein text and find no such disclosure. Additionally, the Office Action does not explain where in the Blaimschein disclosure such teaching may be found. Although some may think that it would be obvious to use a variant of the Blaimschein method to efficiently form printed wiring boards from a predetermined manufacturing block, the Office Action does not states that the rejection relies on the above-identified claim feature being an obvious variant for the subject matter taught by Blaimschein. According to the Office Action, the rejection is based on a belief that Blaimschein teaches the claim feature. For at least this reason alone, the rejection is not properly justified.

The Office Action indicates on page 11, last paragraph, that the Blaimschein camera 3 teaches the claimed detecting unit. However, as explained in column 6, lines 13-14 and 32-33, camera 3 detects workpieces (analogous to the predetermined manufacturing blocks) instead of blanks (analogous to the printed wiring boards).

The Office Action also cites element (e) of the Blaimschein claim 1, which recites the following:

> (e) entering the obtained data into a computer having a memory having stored therein data as to number, contour and quality requirements of the blanks, the computer being programmed to compute a pattern on the basis of the entered and stored data.

Although this text may imply that a human operator or an automated process obtains the number of blanks for a pattern on a workpiece, this text does not discuss whether the blanks are "fractional" as claimed. That is, the recited step broadly describes a step of entering data without regard to whether the blanks are fractional, so the obtained data could possibly describe non-fractional blanks, also. Thus, the cited text cannot anticipate the "detecting unit" described in the claims.

For at least the reason that the Office Action does not properly explain how Blaimschein supposedly teaches the claimed detecting unit, the rejection has not been justified. Accordingly, the rejection should be withdrawn for at least this reason.

Nonetheless, even if it were explained how Blaimschein or Kitamura supposedly teaches or suggests the claimed detecting unit, to justify a rejection of the pending claims, an additional explanation is now required that supposedly explains how Blaimschein or Kitamura teaches or suggests a detecting unit that carries out detection by, for each type of ordered printed wiring board: (1) reading out predetermined manufacturing block data from a panelizing data library;

(2) reading out data of a certain type of ordered printed wiring board from a single piece drawing number data library; and (3) virtually laying out the printed wired boards on the predetermined manufacturing block according to the quantity ordered. Applicants submit that neither Blaimschein nor Kalagnanam et al. teaches or suggests the claimed detection.

Accordingly, applicants solicit the withdrawal of the obviousness rejection based on Blaimschein and Kitamura.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as anticipated by Turner et al. (U.S. Patent No. 6,470,228). Applicants respectfully traverse this rejection as unjustified.

As noted above, claim 1 describes a manufacturing system that includes:

> a detecting unit detecting a plurality of fractional printed wiring boards ... to be laid out to a format of a single predetermined manufacturing block together with a plurality of printed wiring boards having a different type ...

For multiple reasons, applicants assert that the Office Action does properly explain how Turner et al. supposedly teaches a manufacturing system having this element, so the rejection is not justified. Some of the reasons are as follows:

First, applicants respectfully disagree with the statement in the Office Action (page 14, paragraph n) that Turner et al. discloses an element detecting information regarding printed circuit boards. Applicants have searched the Turner et al. text electronically and find no such disclosure of printed circuit boards. Although one might think that it would be obvious to use a variant of the Turner et al. system to manufacture printed wiring boards, the rejection is based on anticipation instead of obviousness. For at least this reason alone, the anticipation rejection is not properly justified.

Also, the rejection relies on inventory information 30 to teach a "detecting unit" as claimed. However, clearly mere data, such as inventory information, is not an element that can

perform the "detecting" function as described in the claim. This is another reason that the rejection is not properly justified.

Further, even if it could be explained how Turner et al. supposedly teaches the claimed detecting unit, to justify an anticipation rejection of the pending claims, an additional explanation is now required that supposedly explains how Turner et al. supposedly teaches a detecting unit that carries out detection by, for each type of ordered printed wiring board: (1) reading out predetermined manufacturing block data from a panelizing data library; (2) reading out data of a certain type of ordered printed wiring board from a single piece drawing number data library; and (3) virtually laying out the printed wired boards on the predetermined manufacturing block according to the quantity ordered. Applicants submit that Turner et al. does not teach the claimed detection.

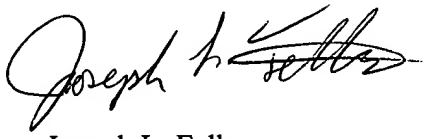
Accordingly, applicants solicit the withdrawal of the anticipation rejection based on Turner et al.

In a separate matter, claims 9 and 10 are amended to recite the terms "printed wiring board data" and "predetermined manufacturing block data" analogously to the recitation in claim 1. (The amendment was inadvertently omitted from applicants' February 17, 2004 submission to the PTO.)

In view of the remarks above, applicants now submit that the application is in condition for allowance. Accordingly, a Notice of Allowability is hereby requested. If for any reason it is believed that this application is not now in condition for allowance, the Examiner is invited to contact applicants' undersigned attorney at the telephone number indicated below to arrange for disposition of this case.

In the event that this paper is not timely filed, applicants petition for an appropriate extension of time. The fees for such an extension, or any other fees which may be due, may be charged to Deposit Account No. 50-2866.

Respectfully submitted,
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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